

2 CHANNEL LOW CAPACITANCE CSP TVS DIODE ARRAY
Product Summary

V _{BR} (Min)	I _{PP} (Max)	C _{I/O} (Max)
6V	5.5A	0.75pF

Description

This new generation TVS is designed to protect sensitive electronics from the damage due to ESD. The combination of small size and high ESD surge capability makes it ideal for use in portable applications such as cellular phones, digital cameras, and MP3 players.

Applications

Typically used at high-speed ports such as USB 2.0, IEEE1394 (FireWire®, iLink), Serial ATA, DVI™, HDMI™, PCI™.

Features

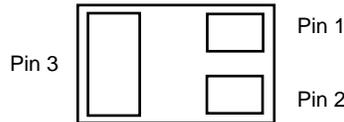
- Clamping Voltage: 9V at 10A 100ns, TLP 9.4V at 5.5A 8µs/20µs
- IEC 61000-4-2 (ESD): Air — ±16kV, Contact — ±16kV
- IEC 61000-4-5 (Lightning): 5.5A (8/20µs)
- 2 Channels of ESD Protection
- Low Channel Input Capacitance of 0.75pF Max
- TLP Dynamic Resistance: 0.25Ω
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

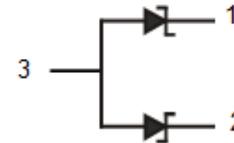
- Case: X3-DSN1006-3 (Type B)
- Case Material: Chip Scale Package
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiAu Bump. Solderable per MIL-STD-202, Method 208
- Weight: 0.001 grams (Approximate)



Top View



Bottom View



Device Schematic

Ordering Information (Note 4)

Product	Compliance	Marking	Reel Size (inches)	Tape Width (mm)	Quantity per Reel
DT1240-02LP10-7B	Standard	MJ	7	8	10,000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information


Top View
Bar Denotes
Pin 1 and Pin 2

MJ = Product Type Marking Code

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Conditions
Peak Pulse Current, per IEC 61000-4-5	I _{PP}	5.5	A	I/O to V _{SS} , 8/20μs
Peak Pulse Power, per IEC 61000-4-5	P _{PP}	55	W	I/O to V _{SS} , 8/20μs
ESD Protection – Contact Discharge, per IEC 61000-4-2	V _{ESD_CONTACT}	±16	kV	I/O to V _{SS}
ESD Protection – Air Discharge, per IEC 61000-4-2	V _{ESD_AIR}	±16	kV	I/O to V _{SS}
Operating Temperature	T _{OP}	-55 to +85	°C	—
Storage Temperature	T _{STG}	-55 to +150	°C	—

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation Typical (Note 5)	P _D	500	mW
Thermal Resistance, Junction to Ambient Typical (Note 5)	R _{θJA}	250	°C/W

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Conditions
Reverse Working Voltage	V _{RWM}	—	—	5.5	V	I _R =1mA, , I/O to V _{SS}
Reverse Current	I _R	—	—	0.5	μA	V _R = 5.5V, I/O to V _{SS}
Reverse Breakdown Voltage	V _{BR}	6	—	—	V	I _R = 1mA, I/O to V _{SS}
Forward Clamping Voltage	V _F	-1.0	-0.85	—	V	I _F = -15mA, I/O to V _{SS}
Reverse Clamping Voltage (Note 6)	V _C	—	9.4	11	V	I _{PP} = 5.5A, I/O to V _{SS} , 8/20μs
ESD Clamping Voltage	V _{ESD}	—	9	—	V	TLP, 10A, tp = 100ns, I/O to V _{SS}
Dynamic Reverse Resistance	R _{DIF-R}	—	0.25	—	Ω	TLP, 10A, tp = 100ns, I/O to V _{SS}
Dynamic Forward Resistance	R _{DIF-F}	—	0.25	—	Ω	TLP, 10A, tp = 100ns, V _{SS} to I/O
Channel Input Capacitance	C _{I/O}	—	—	0.75	pF	V _{I/O} = 2.5V, V _{SS} = 0V, f = 1MHz
Delta C _{I/O}	C _{I/OMAX} -C _{I/OMIN}	—	0.04	—	pF	C _{I/OMAX} -C _{I/OMIN}

Notes: 5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at <http://www.diodes.com/package-outlines.html>.

6. Clamping voltage value is based on an 8x20μs peak pulse current (I_{PP}) waveform.

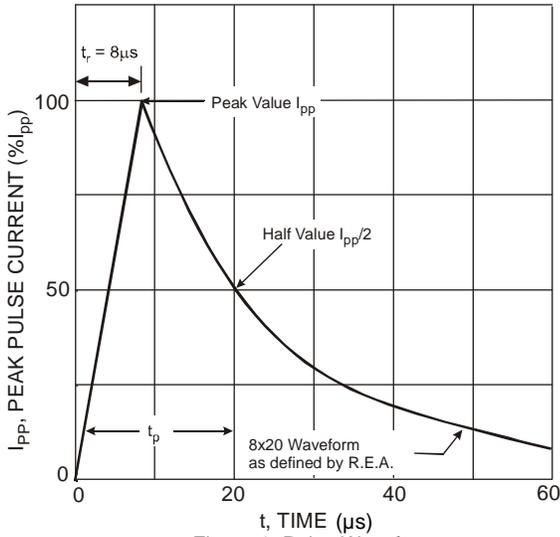


Figure 1 Pulse Waveform

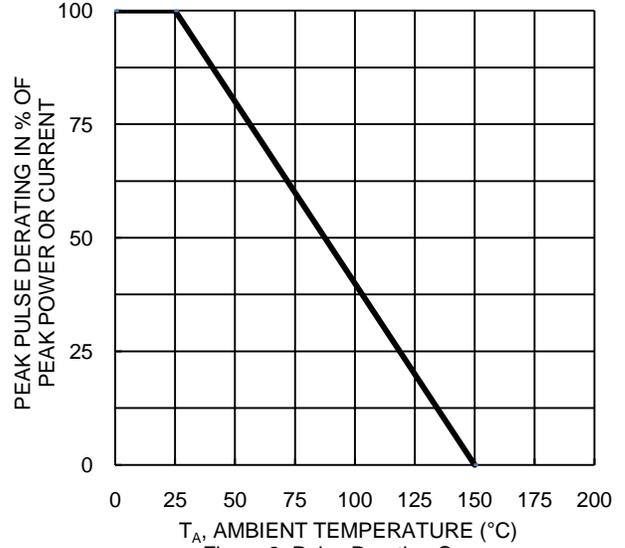


Figure 2. Pulse Derating Curve

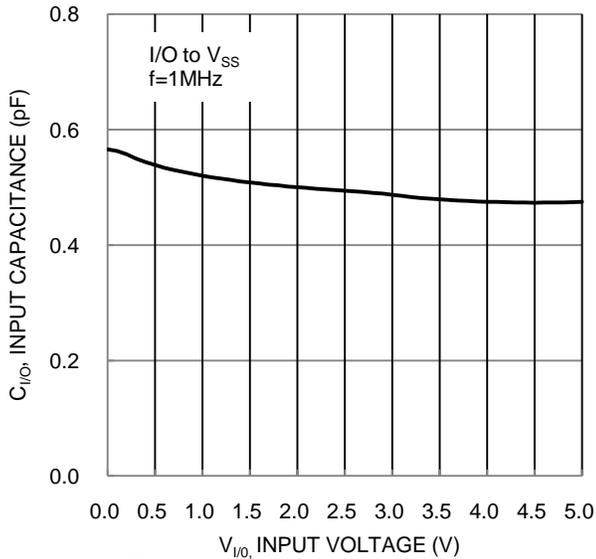


Figure 3. Input Capacitance vs. Input Voltage

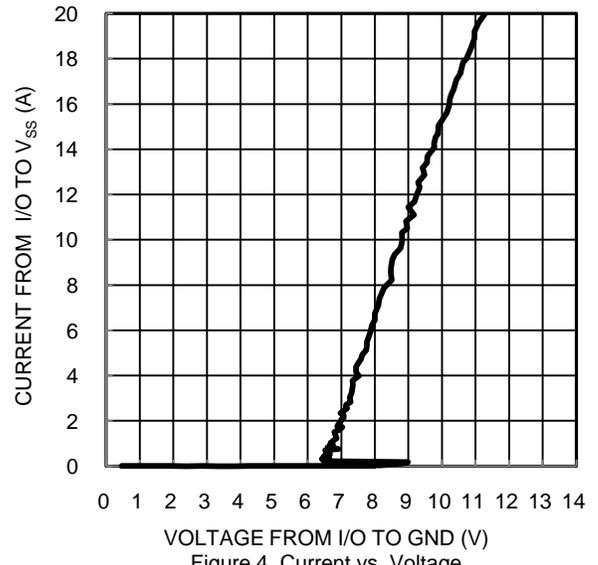
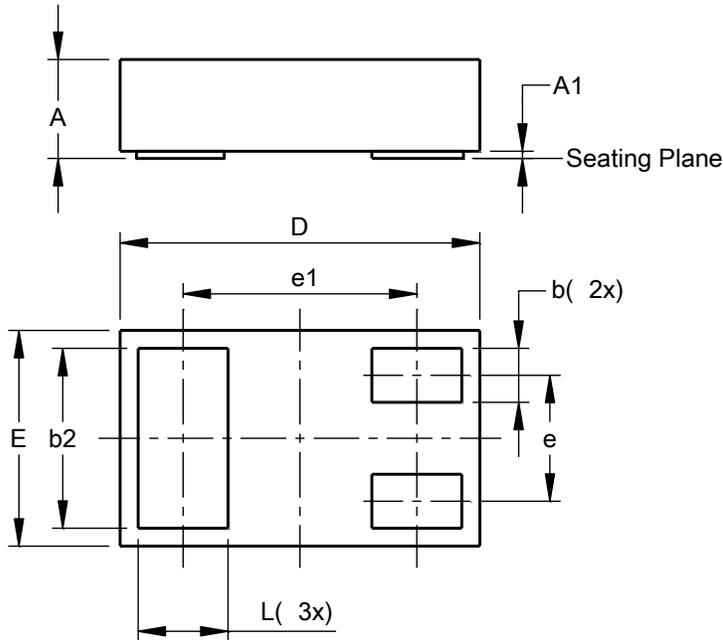


Figure 4. Current vs. Voltage

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X3-DSN1006-3 (Type B)



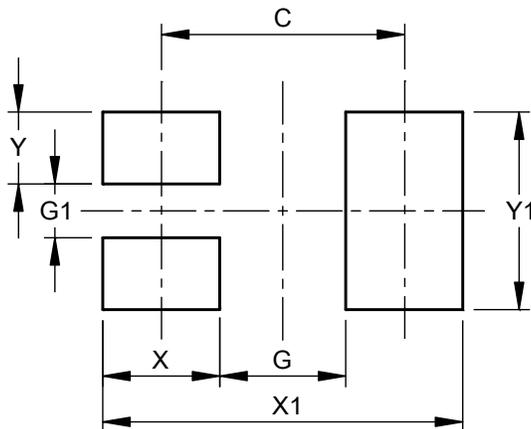
X3-DSN1006-3 (Type B)			
Dim	Min	Max	Typ
A	0.250	0.300	0.275
A1	0.00	0.02	0.01
b	0.130	0.170	0.150
b2	0.480	0.520	0.500
D	0.975	1.025	1.00
E	0.575	0.625	0.600
e	--	--	0.350
e1	--	--	0.650
L	0.230	0.270	0.250
All Dimensions in mm			

Note 7: Device side walls are electrically active bare silicon. Avoid contact of solder or flux on the side walls during the PCB assembly process.

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X3-DSN1006-3 (Type B)



Dimensions	Value (in mm)
C	0.70
G	0.30
G1	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

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